Design of Fast and Area Efficient Fault Tolerant Parallel FFTs using Partial Summation ECC

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Abstract – The increasing demand of low complexity and error tolerant design in signal processing systems is a reliability issue at ground level. The complexity of communications and signal processing circuits increases every year which is done by the CMOS technology scaling. This increased complexity makes the circuits more vulnerable to errors. As soft errors pose reliability threat to modern electronic circuits, it becomes necessary to protect circuits against soft errors. The ABFT techniques are well suited for communications and signal processing applications as they use algorithmic properties to detect and correct errors. One example is FFT. In this brief, ECC technique is first applied to protect parallel FFTs, then Parity-SOS and Parity-SOS-ECC techniques are applied. Then, an improved protection scheme that combine the use of error correction codes and Parseval sum is proposed and evaluated. The results show that the proposed scheme can reduce the implementation cost of protection.

Index Terms— Error correction codes, (ECCs), fast Fourier Transforms (FFTs), soft errors, Partial Summation.

1. INTRODUCTION

This increased complexity makes the circuits more susceptible to errors. This is made possible by the CMOS technology scaling that enables the integration of more and more transistors on a single device. At the same time, the scaling means that transistors operate with lower voltages and are more vulnerable to errors caused by noise and manufacturing variations. The meaning of radiation-induced soft errors also increases as technology scales. Soft errors can change the logical value of a circuit node creating a temporary error that can affect the system operation.

Many techniques have been proposed to ensure that soft errors do not affect the operation of given circuit. These contain the use of special manufacturing processes for the integrated circuits like, for example, the silicon on insulator. Another option is to design basic circuit blocks to minimize circuit the probability of soft errors. It is also possible to add redundancy at system level. One example is Triple modular Redundancy (TMR). It triples a block and votes among three outputs to detect and correct errors. TMR technique requires large overhead in terms of circuit implementation. Another approach is to use algorithmic properties of the circuit commonly called as Algorithmic-based fault tolerance (ABFT). Over the years, many ABFT techniques have been planned to protect the basic blocks that are commonly used in those circuits. Some works have considered the protection of digital filters. There are four main contributions in this brief:

- The evaluation of the ECC technique for the protection of parallel FFTs showing its effectiveness in terms of overhead and protection effectiveness.
- A technique based on the use of Parseval or sum of squares (SOSs) checks combined with a parity FFT.
- A technique on which the ECC is used on the SOS checks instead of on the FFTs.
- The proposed technique: Parity-Partial Summation-ECC.

2. RELATED WORK

The parallel FFTs are protected using different techniques, each of which uses its algorithmic properties.

2.1 Parallel FFT Protection Using ECC Technique

This technique provides new alternatives to protect parallel FFTs that can be more efficient than protecting each of the FFTs independently. This is based on the protection scheme based on the use of ECCs that was presented in for digital filters[2].This scheme is shown in Fig1. In this example, a simple single error correction Hamming code[3] is used. The original system consists of four FFT modules and three redundant modules is added to detect and correct errors. The inputs to the three redundant modules are linear combinations of the inputs and they are used to check linear combinations of the outputs.

For example, the input to the first redundant module is $x_5=x_1+x_2+x_3$.

and since the DFT is a linear operation, its output z_5 can be used to check that

$z_5 = z_1 + z_2 + z_3$

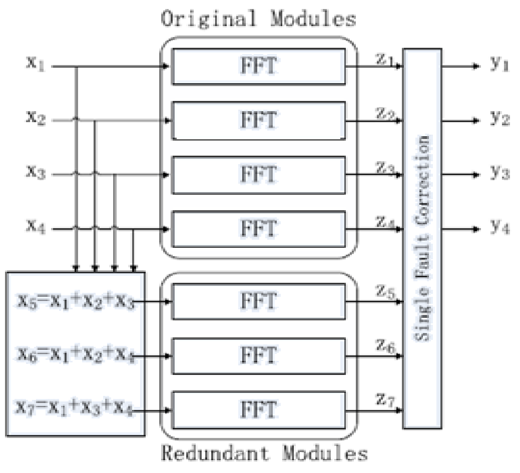

Fig. 1. Parallel FFT protection using ECCs

$c_1c_2c_3$	Error Bit Position
000	No error
111	z_1
110	z_2
101	z_3
011	z_4
100	z_5
010	z_6
001	z_7

Table 1: Error location in the hamming code.

This will be denoted as c1 check. The same reasoning applies to the other two redundant modules that will provide checks c2 and c3.Based on the differences observed on each of the checks, the module on which the error has occurred can be determined. The different patterns and the corresponding errors are summarized in Table1. Once the module in error is known, the error can be corrected by reconstructing its output using the remaining modules. For example, for an error affecting z1, this can be done as follows:

$z_{1c}[n] = z_5[n] – z_2[n] – z_3[n]$

The overhead of this technique is lower than the TMR as the number of redundant FFTs is related to the logarithm of the number of original FFTs.

2.2 Parallel FFT Protection Using Parity-SOS Technique

Over the years, many techniques have been proposed to protect the FFT. One of them is the Sum of Squares (SOSs) check that can be used to detect errors. The SOS check is based on the Parseval theorem that states that the SOSs of the inputs to the FFT are equal to the SOSs of the outputs of the FFT except for a scaling factor. This relationship can be used to detect errors with low overhead as one multiplication is needed for each input or output sample (two multiplications and adders for SOS per sample.

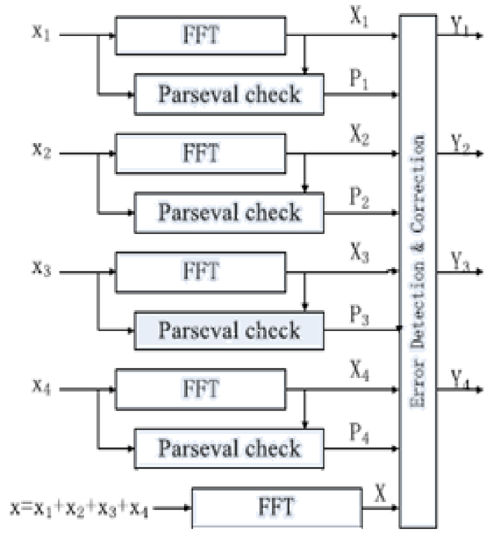

Fig. 2. Parity-SOS fault-tolerant parallel FFTs.

For parallel FFTs, the SOS check can be combined with the ECC approach to reduce the protection overhead. Since the SOS check can only detect errors, the ECC part should be able to implement the correction. This can be done using the equivalent of a simple parity bit for all the FFTs. In addition, the SOS check is used on each FFT to detect errors. When an error is detected, the output of the parity FFT can be used to correct the error.

This is better explained with an example. In Fig. 2, the first proposed scheme is illustrated for the case of four parallel FFTs. A redundant (the parity) FFT is added that has the sum of the inputs to the original FFTs as input. An SOS check is also added to each original FFT. In case an error is detected (using *P*1, *P*2, *P*3, *P*4*)*, the correction can be done by recomputing the FFT in error using the output of the parity FFT(*X*) and the rest of the FFT outputs. For example, if an error occurs in the first FFT, *P*1 will be set and the error can be corrected by doing

$X_{1c} = X – X_2 – X_3 – X_4.$

This combination of a parity FFT and the SOS check reduces the number of additional FFTs to just one and may, therefore, reduce the protection overhead. In the following, this scheme will be referred to as parity-SOS.

The implementation of SOS check is done as:

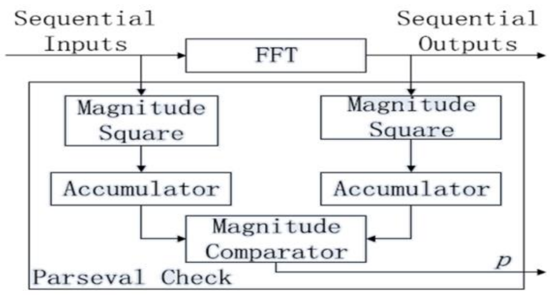

Fig 3: Implementation of SOS check

2.3 Parallel FFT Protection Using Parity-SOS-ECC Technique

Another technique is to combine the SOS check and the ECC approach.

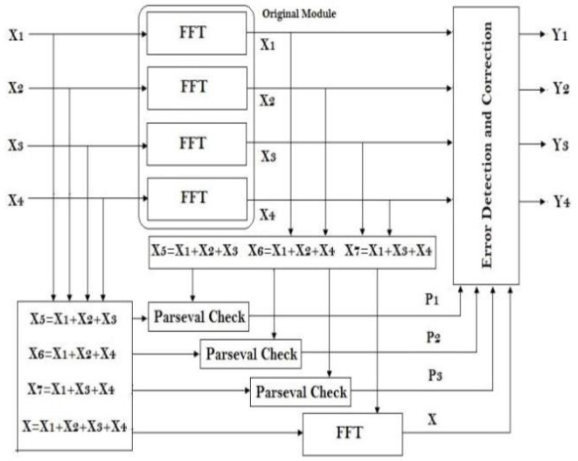

Fig.4:Parity-SOS-ECC fault tolerant parallel FFTs.

Instead of using an SOS check per FFT, use an ECC for the SOS checks. Then as in the parity-SOS scheme, an additional parity FFT is used to correct the errors. This technique is shown in Fig. 3. The main benefit over the first parity- SOS scheme is to reduce the number of SOS checks needed. The error location process is the same as for the ECC scheme in Fig. 1 and correction is as in the parity-SOS scheme. In the following, this scheme will be referred to as parity-SOS-ECC.

3. PORPOSED MODELLING

Parallel FFTs protection is done using Parity-PS-ECC technique. The proposed work focuses on two new techniques for reducing the hardware overhead. Instead of using Sum of Squares, Partial summation is used. Fig 4 illustrates the Parity Partial Summation block for less error prone applications. Here partial summation is not directly applied to the input and output of FFTs. Using partial summation, syndromes will be generated. The syndrome generated is used to detect the fault and a redundant FFT is used to correct the fault.

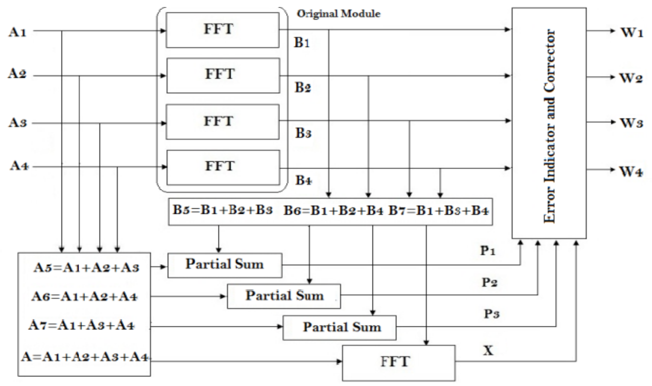

Fig 5: Parity-PS-ECC fault-tolerant parallel FFTs

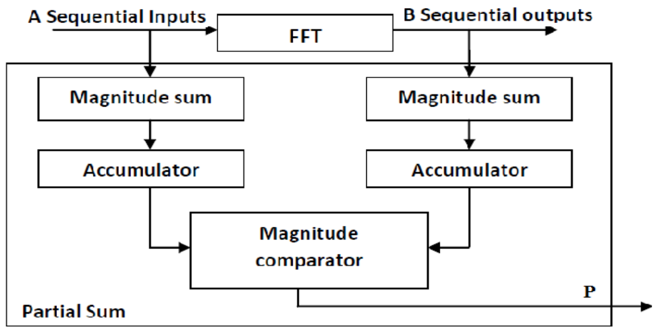

Fig 6: Implementation of Partial Summation

Fig 6 shows implementation architecture of partial summation block. The sequential input and output of the 4-point FFT is fed to the magnitude sum block. The magnitude comparator compares the input and output for verifying the FFT output. If both are equal then the FFT is soft error free.

	FFTs	**SOS checks**	**Partial-sum**
ECC	$1+\log_2(k)$	0	0
Parity-SOS	1	k	0
Parity-SOS-ECC	1	$1+\log_2(k)$	0
Parity–PS-ECC	1	0	1+log2(k)

Table 2: Overhead of the different schemes to protect *k* FFTs

4. RESULTS AND DISCUSSIONS

The proposed scheme has been implemented on an FPGA and evaluated both in terms of overhead and power. A four-point decimation-in-frequency FFT core is used to compute the FFT iteratively. This core has been developed to implement MIMO-OFDM for wireless systems. The FFT and the different protection techniques have been implemented using Verilog. The parity-PS –ECC technique has the lowest resource use in all cases and, therefore, is the best option to minimize the implementation cost.

Design Summary	ECC	Parity-SOS	Parity-SOS-ECC	Parity-PS-ECC
slices	126	116	90	73
Flipflops	48	33	27	24
LUTs	208	194	161	127
Delay(ns)	4.629	13.929	17.26	3.368

Table 3: Resource utilization for 4 parallel FFTs

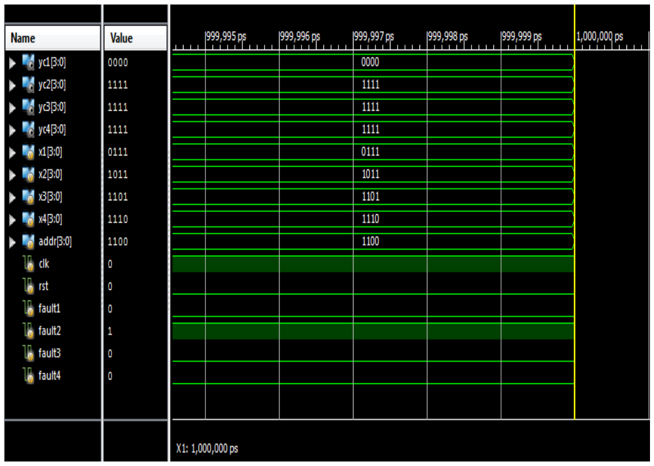

Fig 7: Simulation results for Fault-Tolerant Parallel FFTs protection using ECC.

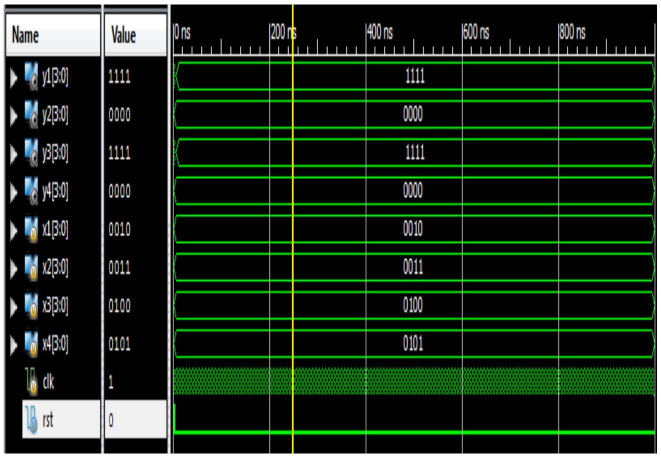

Fig 8: Simulation Results for Parity - SOS Fault-Tolerant Parallel FFTs.

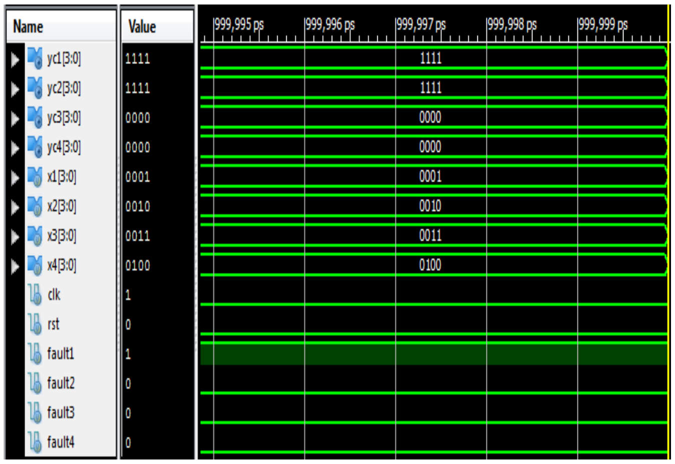

Fig 9: Simulation Results for Parity-SOS-ECC Fault-Tolerant Parallel FFTs

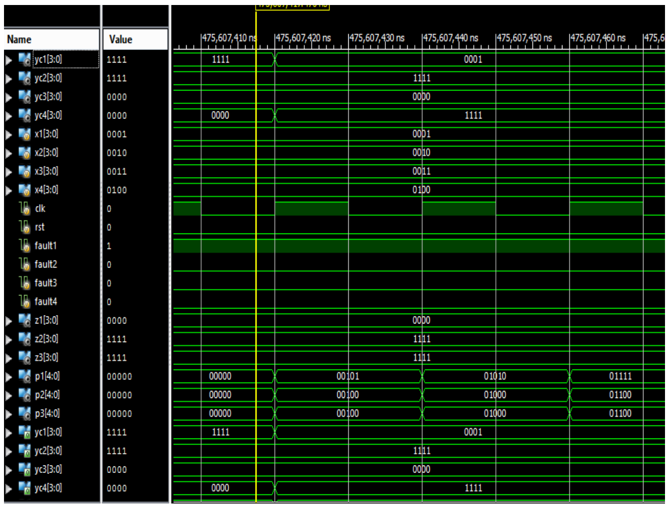

Fig 10: Simulation Results for Parity-PS-ECC Fault-Tolerant Parallel FFTs.

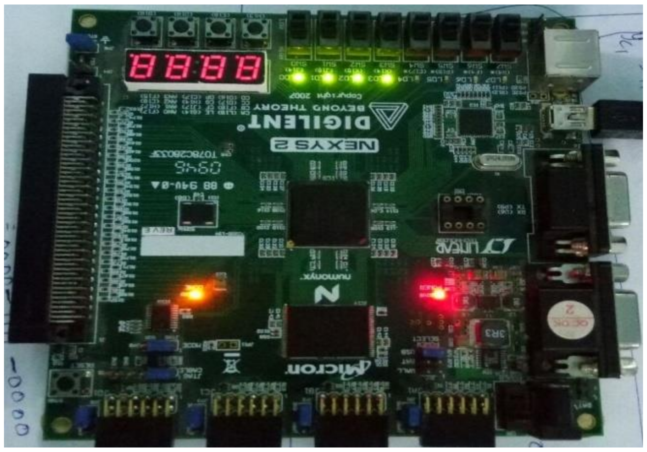

Fig 11: Corrected output for the Parity-PS-ECC (proposed technique).

5. CONCLUSION

The protection of parallel FFTs implementation against soft errors has been studied. A technique has been proposed and evaluated. The proposed technique is based on combining error correction codes and partial summation. The proposed techniques have been evaluated both in terms of implementation complexity and speed (delay). The results show that the proposed technique, which uses a parity FFT and a set of Parseval Summation checks that form an ECC, provides the best results in terms of implementation complexity and has low power consumption.

In the future work, self adaptive systems to overcome hard errors can also be taken into consideration.

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